Contents

1. ESD — A New EMI Environment 805
2. ARC Source 808
3. ESD Testing 810
4. Summary 813

8. Plasma Charging Testing of Communication Satellites

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Abstract

This paper discusses ESD as a radiated electromagnetic environment and compared the ESD environment to "standard" EMI test environment. An arc generator ueed to assess th&sensitivity of typical spacecraft electronics is described.

The results of radiated susceptibility test$ conducted on breadboard circuits and a satellite electrical model of a communication satellite are discussed.

1. ESD - A NEW EMI ENVIRONMENT

EMC requirements €or communication satellites built at GE Splice Division specify the test requirements of MIL-STD-461 arid the test levels of MIL-STD-462 tailored to the specific mission. The radiated susceptibility tests typically specified are RS02 and RS03.

RS02 (see Figure 1) is a low frequency magnetic susceptibility test. A wire id wrapped around the harness of the unit urider test and the voltage spike in Figure 1 is impressed on a 10 ohm resistor.

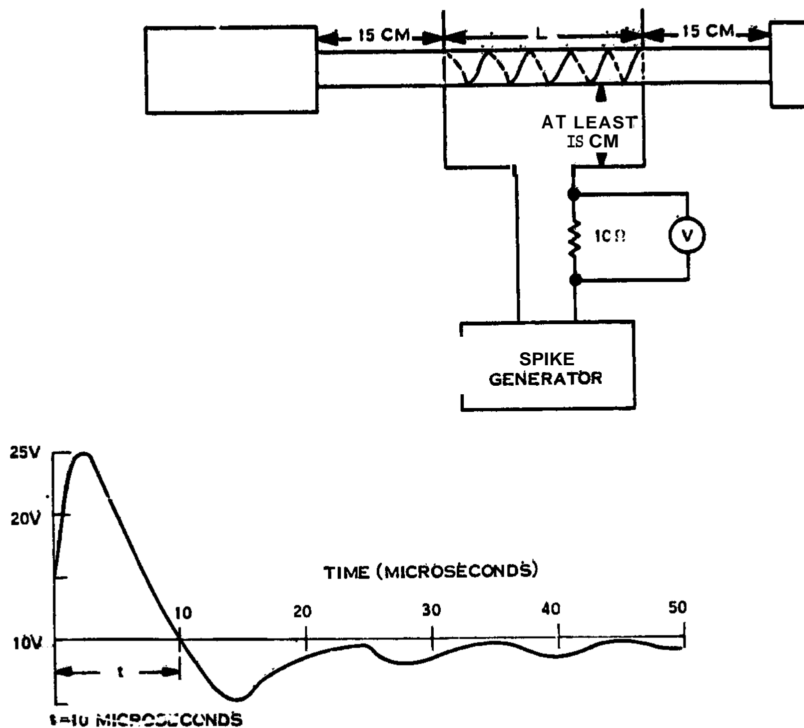


Figure 1. RS02

RS03 is a wideband electric field sensitivity test. The test is performed with a series of antennas and oscillators to cover the spectrum shown in Figure 2.. The test oscillator is swept so that only one frequency at a time is applied to the test sample. The peaks in the spectrum correspond to the frequencies of on board transmitters.

Recognition of the plasma charging phenomena and the accompanying arc discharge results in a different EMI phenomena – high level radiation With frequency components extending from the low kilohertz to the gigahertz region.

Figure 3 illustrates the spectrum of a trapazoidal pulse with a 15-nsec rise time, a 40-nsec pulse width, and a peak amplitude of 1260 V/M. A significant difference between the curves of Figure 2 and Figure 3 is that the frequencies in Figure 3 are radiated simultaneously, while those of Figure 2 are radiated discretely.

This environment hhd not been previously teated at GE Space Division. A test program was instituted to assess the arc vulnerability of typical circuitry designed tb tailored 462 levels and standard EMC practices, thht is:

(1) Minimize circuit bandwidth.

(2) Use twisted pair wiring and differential techniques fbr low level signals.

(3) All boxes well bonded to structure.

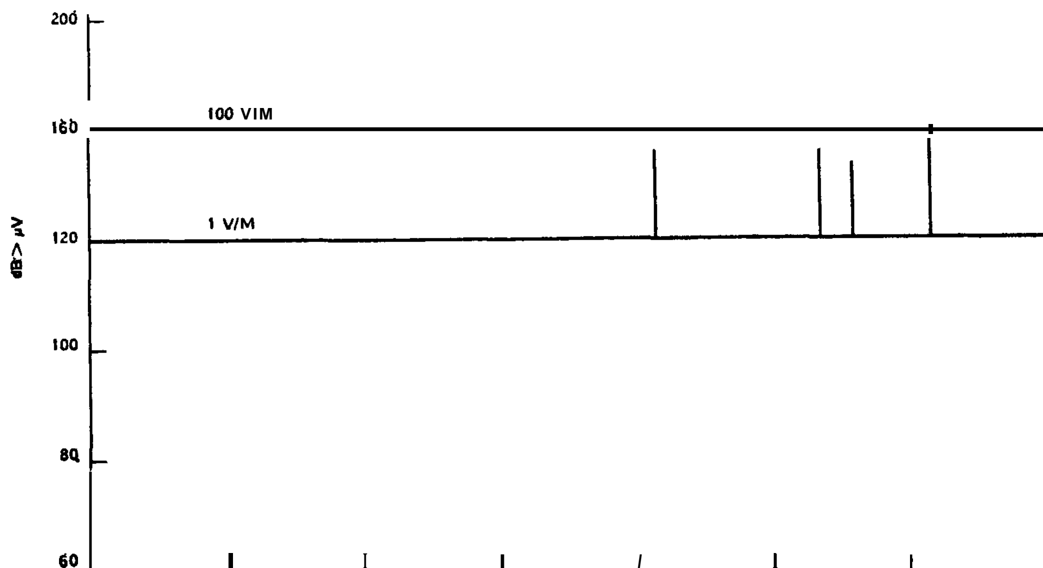
The objectives of the tes' ; were:

(1) To determine if the arc was destructive to spacecraft circuitry.

(2) To establish upset levels of digital interface circuits.

(3) To establish response thresholds of analog circuits.

(4) To determine if "latch-up" modes Were excited when IC inputs were pulled above and below the supply voltages.



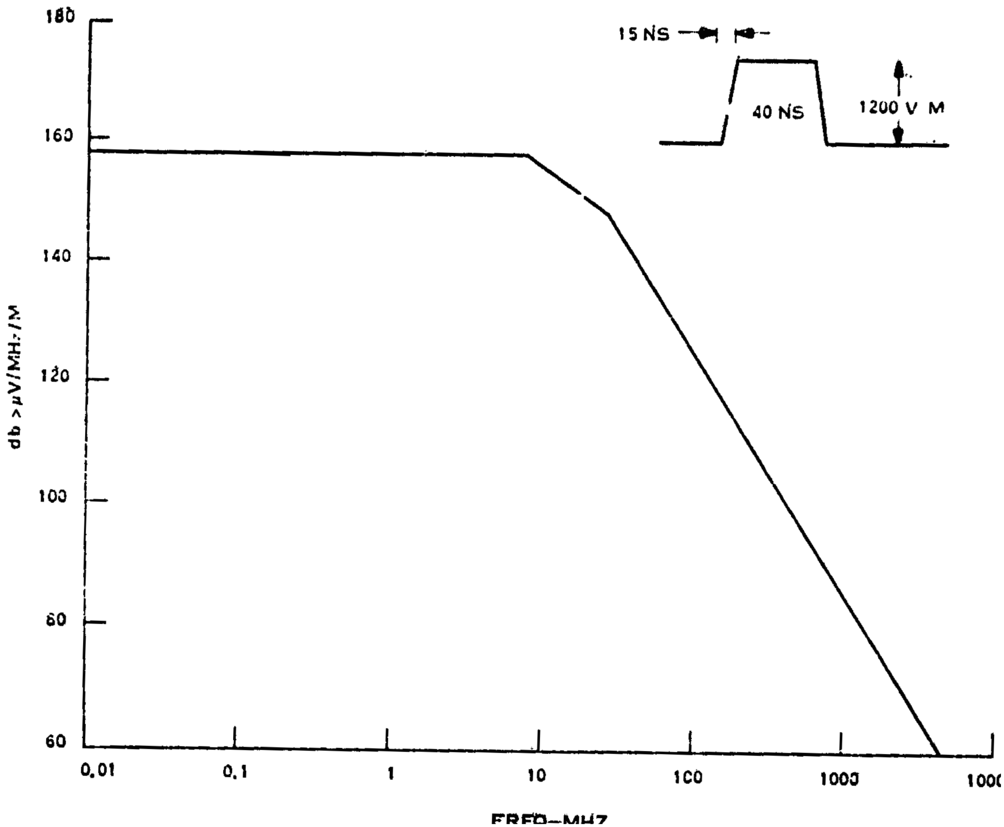


Figure 3. ARC Spectrum

2. ARC SOURCE

Since the plasma charging environment is not well defined, specification of a suitable arc source required engineering judgement. The arc source fabricated was based on a NASA approach and was similar to an arc source used during CTS testing, A block diagram of the arc generator is shown in Figure 4. A high voltage power supply charged the capacitor C through resistor R1. When the capacitor voltage reached the tube breakdown voltage, the capacitor discharged through R2 and the tube. The tube, capacitor, and resistors were easily changed so the breakdown voltage ahd arc energy were easily varied. A picture of the arc generator is shown in Figure 5.

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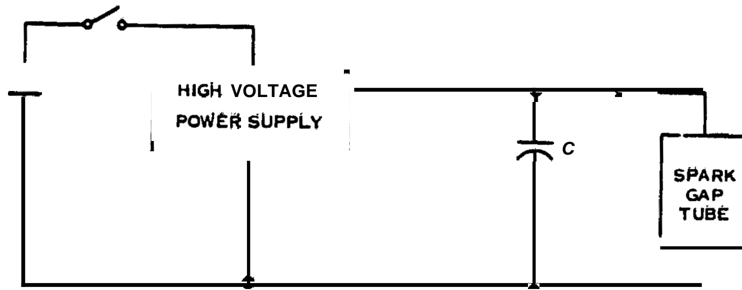


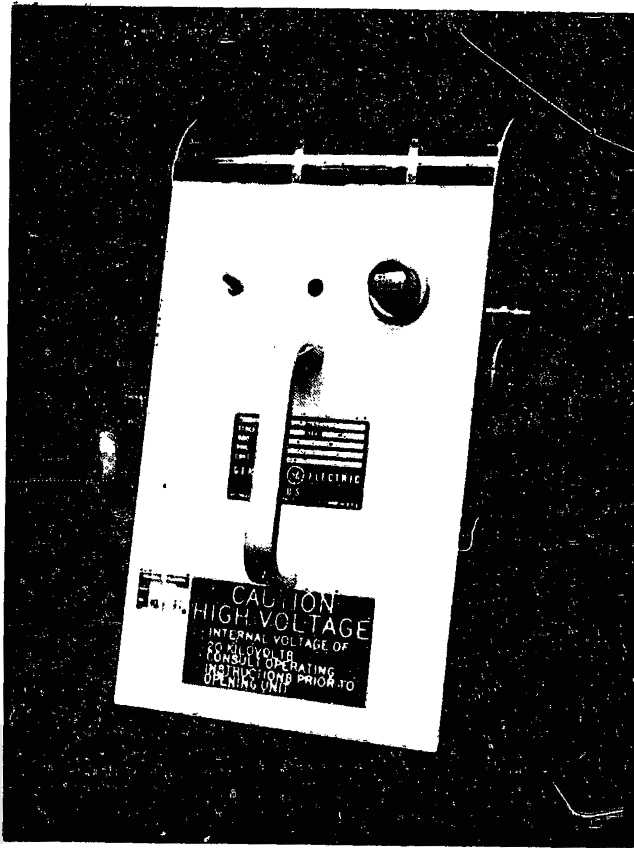


Figure 5. ARC Generator

3. ESD TESTING

3.1 Circuit Testing

The testing proceeded in two phases, In the initial phase, breadboards of typical spacecraft circuits judged to be most sensitive to ESD were fabricated. The circuit test setup was a shdwn in Figure 6. The test circuits were located outside of the screen room and the arc generator was inside?the screen room. The test procedure was tb mbve the arc generator progressively closer to the test harness and to observe circuit performance. This test approach assumed the component boxes were Well sealed and the harness was unshielded. The wires in the screen room were routed 5 cm above the ground plane and were radiated by the arc generator at distances of 30 cm to 2 cm. Test levels fbr the breadboard testing Were set at 10 kV and 36 mJ.

The first circuit tested wad the analog telemetry Conditioning circuit shown in Figure 7. The 100 ohm resistor simulates a temperature sensor arid the 1 MΩ resistor simulates a telemetry encoder input resistance. The encoder is vulnerable because of the high resistance single-ended interface. In operation, a low bandwidth sample and hold circuit is usually incorporated in the encoder to minimize high frequency pickup. The voltage induced at various test paints was photographed as the arc generator was moved from 30 cm to 2 cm. Only one wire Was in the screen room at a time. The induced voltage was an exponentially damped sine wave lasting approximately 400 nsec. The chart in Figure 7 indicates the maximum peak-to-peak voltage induced when AD was in the screen room. Similar irradiating of the 100 ohm resistor resulted in 110 volts peak-to-peak at 2 cm at the bridge input. In all cases there was no damage and no circuit latch up. The high voltages induced in the 1 MΩ resistor indicated that damage ti, a telemetry encoder was possible.

The next circuit tested was a digital interface shown in Figure 8. The twisted pair interconnecting harness was radiated at distances from 30 cm to 2 cm. The induced voltage again was 20 MHz with a 40b nsec duration. The maximum peak-to-peak voltage is shown in the chart on Figure 8. At distances to ? cm there Was no circuit malfunction. At 2 cm the circuit malfunctioned. Considering the + input of the LM 199 receiver, the negative excursion of the! ringing was clamped by the diode across the 100k resistor; however, the positive excursion of the ringing pulled the + input above the supply voltage and excited a parasitic mode, The receiver was upset for 400 used. The rekelver was not damaged and subsequently functioned normally. Wrapping the harness with 3 mil copper foil reduced the ringing amplitude at G to 45 volts and eliminated the spurious response.

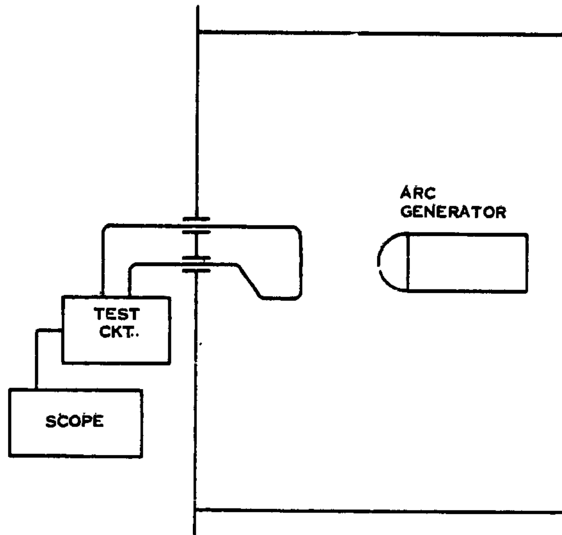


Figure 6. Circuit Test Setup

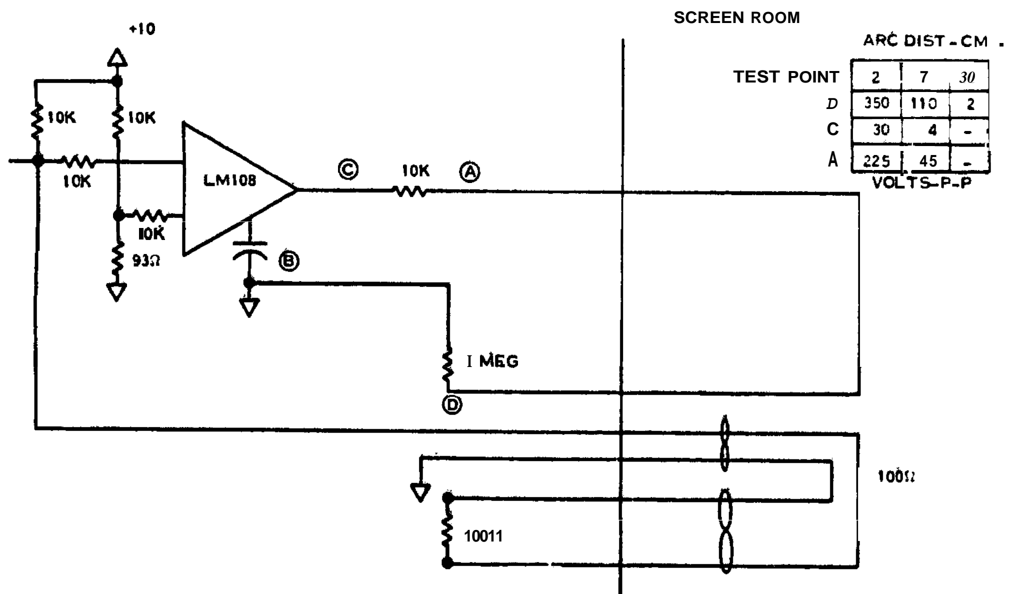
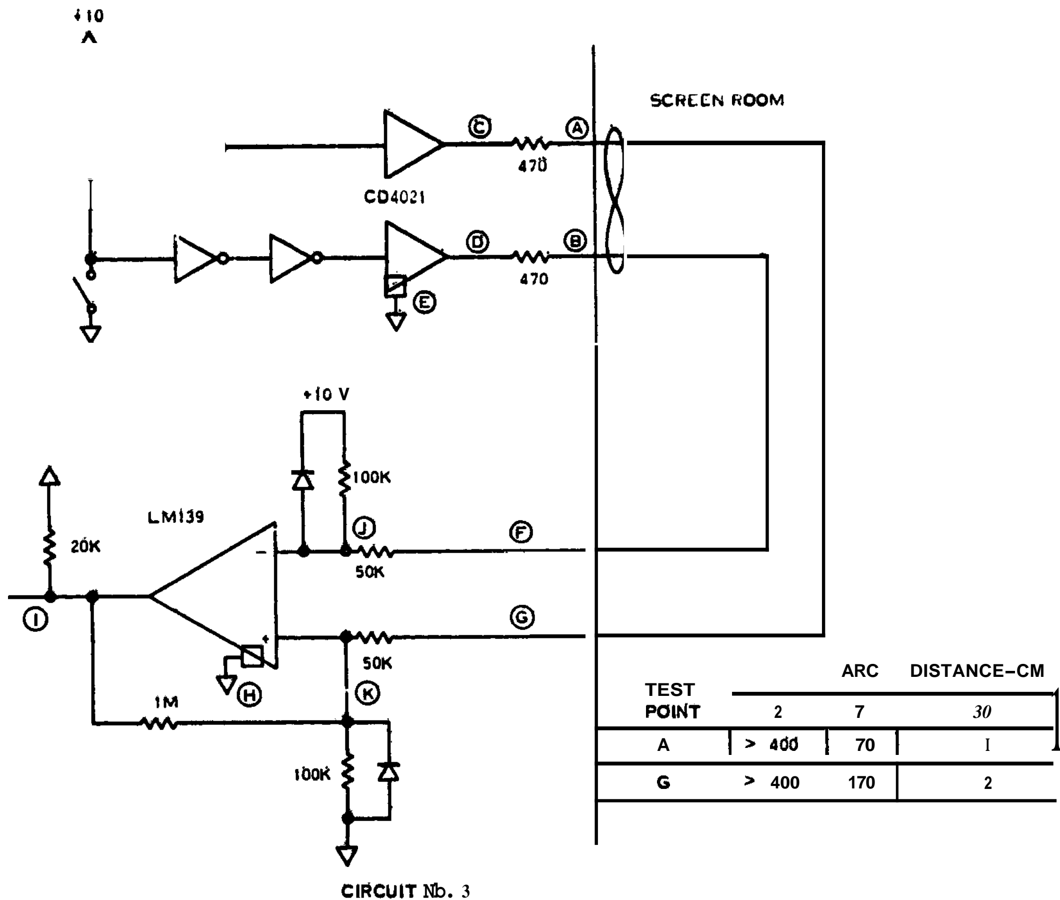


Figure 7. Analog TLM Conditioner CKT



TEST POINT	ARC DISTANCE-CM		
	2	7	30
A	> 400	70	I
G	> 400	170	2

Figure 8. Digital Interface CKT

3.2 Satellite Electrical Model Testing

After completion of the breadboard tests, a test was conducted on a satellite electrical model of a communication satellite currently under development. Figure 9 is a diagram of a typical satellite electrical model. These models are built with engineering model components. The harness is flight-like, but is unshielded. A heavy sheet of aluminum foil is mounted on the underside of the table and all boxes are electrically bonded to the ground plane. Performance of the satellite electrical model is monitored via a telemetry link to a test ground station. The test procedure was to radiate all harness segments, box interface connectors, and box surfaces at distances from 30 cm to 2 cm. The arc source was set at 13 kV and 455 mJ.

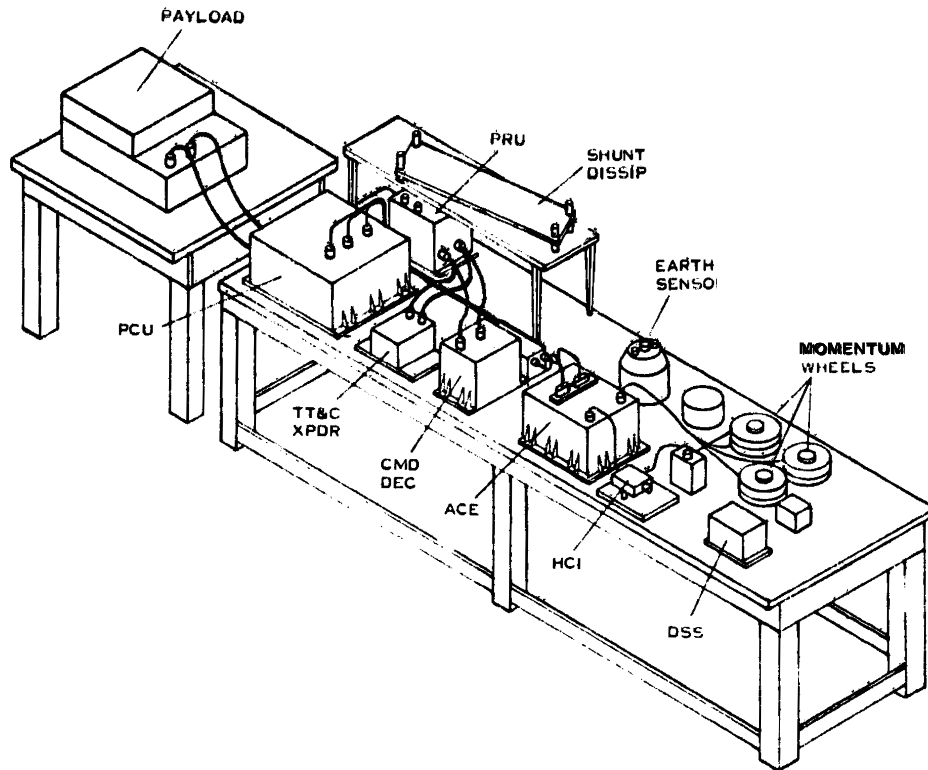


Figure 9. Typical Satellite Electrical Model

When the arc source was more than 7 cm from the hardware, there was no noticeable effect on system performance. At 2 cm the telemetry encoder lost frame sync. There was no upset of the serial digital interface circuit. This was attributed to the shielding effect of other wires in the harness bundle. Transient anomalies were recorded on two telemetry readings. The command system was unaffected at 2 cm arc distance. The PIN diodes in the transponder experienced a transient gain change, but quickly returned to normal operation.

4. SUMMARY.

At arc distances greater than 7 cm, there was no effect on circuit or electrical satellite model performance. At 2 cm, upsets but no damage was experienced. The testing was severe; however, there is no assurance that we over-tested. Clearly, the efforts to understand and characterize the charging phenomena must continue so that meaningful test levels can be established.