IMPROVED DEMONSTRATION OF INTERNAL CHARGING HAZARDS USING THE 'REALISTIC ELECTRON ENVIRONMENT FACILITY' (REEF)

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Abstract

Experimental ground testing has been carried out to determine whether digital latches can spontaneously change state in severe (space weather induced) outer-belt environments via the mechanism of internal spacecraft charging/discharging. A new facility is employed which improves simulations of the charging environment experienced by satellite equipment and materials. Results are presented which demonstrate the complete chain of events from environment to circuit anomaly. The anomaly rate shows dependence on both charging flux and circuit board temperature.

Introduction

Numerous spacecraft anomalies in the outer radiation belt have been attributed to electrostatic discharges (ESD) resulting from internal charging [1,2]. Charging occurs when intense fluxes of energetic electrons, typical of the outer belt, penetrate spacecraft shielding and are deposited in dielectrics or isolated metal components. Over periods of days, the build up of charge can result in intense electric fields and eventual ESD. This can induce a current 'spike' in electronic components resulting in upset or damage. Although there is convincing in-orbit evidence for a link between internal charging and spacecraft anomalies it is essentially circumstantial – for example anomalies are often seen to coincide with periods of enhanced electron flux. So far, laboratory simulations [3, 4, 5] and flight experiments [6, 7] have tended to concentrate on the charging process or ESD events *per se* rather than demonstrating their effect on electronics. As a result the complete chain of cause and effect (environment $\Rightarrow$ internal charging $\Rightarrow$ ESD $\Rightarrow$ electronic upset) has not been fully demonstrated leading to residual scepticism in some quarters about the reality of such effects [7]. The work presented here examines the behaviour of a digital electronic circuit while subjected to improved simulations of the environment experienced by electronic equipment in GEO. The basic approach is the irradiation of active circuit boards with an electron 'beam' well matched in intensity and spectrum to outer belt conditions. Observation of the behaviour

of the active circuit has been undertaken, as well as monitoring for discharges in general. The prime benefits of the study are:

- accurate simulation of on-orbit environmental conditions over long periods (days or even weeks);
- use of space-approved materials, components and structures;
- use of representative electronic circuits.

The Realistic Electron Environment Facility (REEF)

A high degree of realism was a basic aim of this work in order to properly simulate internal charging effects. Therefore a good simulation of the outer belt energetic electron spectrum was essential. While such simulations are available from some electron beam facilities [e.g. 5] via use of scattering foils, these facilities do not readily offer the capability to carry out very long duration testing, nor the ability to maintain and vary sample temperatures.

To undertake this work a new 'Realistic Electron Environment Facility' (REEF), was developed. REEF consists of a vacuum chamber ($<10^{-5}$ m bar) containing a ^{90}Sr source and the item under test. The temperature of the sample is maintained by coupling it to a thermally controlled plate. The plate's temperature can be stabilised to better than 1°C and controlled over the range -10°C to +40°C; this is important as the conductivity of dielectrics, and therefore the rate at which trapped charge will leak away, is strongly temperature dependent [8].

It was decided to use ^{90}Sr (a pure β-emitter) to simulate the space electron environment since it offers a number of advantages over conventional electron beams for this application and these are summarised in Table 1.

Sr90 source	Electron beam facility
spectrum is a good match to typical outer belt spectra from 0.1MeV up to 2.2MeV	mainly mono-energetic
current intensities can be made comparable to the worst-case GEO environment	minimum beam intensity is usually too high
spectrum is accurately known and fully repeatable between different laboratories the half life is 28 years and so the emission characteristics will be stable over long periods	at low currents, beam current variability over long periods can be significant
relatively small running costs are involved and long term testing is feasible	generally expensive to rent cannot readily be run continuously beyond one working day

Table 1. The advantages of 90Sr facility over an electron beam

The electron flux (usually quoted in terms of current density, pA/cm^2) at the sample can be altered by variation of source-sample distance. Integral spectra for the maximum and minimum source-sample distances possible within REEF are shown in Fig. 1 together with the average GEO electron environment from the NASA AE8 average model [9], the NASA Spacecraft Charging Handbook severe-case spectrum [10] and a 'worst-case' GEO environment predicted by the FLUMIC model [11]. FLUMIC is used in ESA's DICTAT internal charging analysis tool [12]. It can be seen that the REEF capability brackets the predicted GEO levels and provides a good spectral match up to approximately 2MeV.

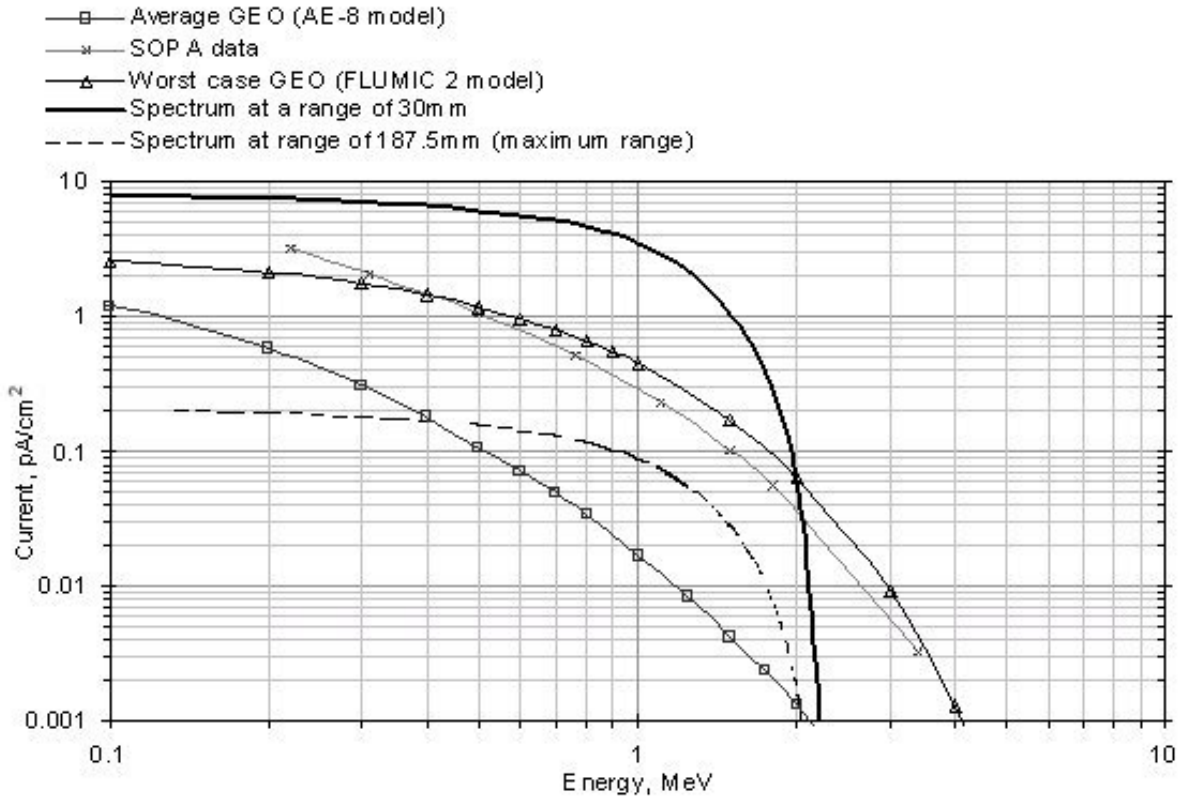

Figure 1. Integral electron spectra in REEF at the maximum and minimum source-sample distances compared with predicted worst-case and average GEO environments.

The electron current density at the sample varies approximately as the inverse square of the source-sample distance, except at very small distances where the finite source size (~5mm) makes the decrease somewhat slower.

The REEF spectra presented in Fig. 1 depict electron currents on the beam axis, but off-axis the current seen by a flat sample will decrease due to both the increased distance from the source and the oblique irradiation angle which results in unit sample area having a reduced effective area to collect current. This off-axis decrease has been measured and results are shown in Fig. 2 out to a radial distance of 40mm for source-sample distances of 37mm and 77mm. As would be expected the 'beam' is far more uniform at the larger source-sample distance; this may be important where uniform irradiation of a sample is critical. The electron flux can be reduced to zero by closing a shutter in front of the source when required.

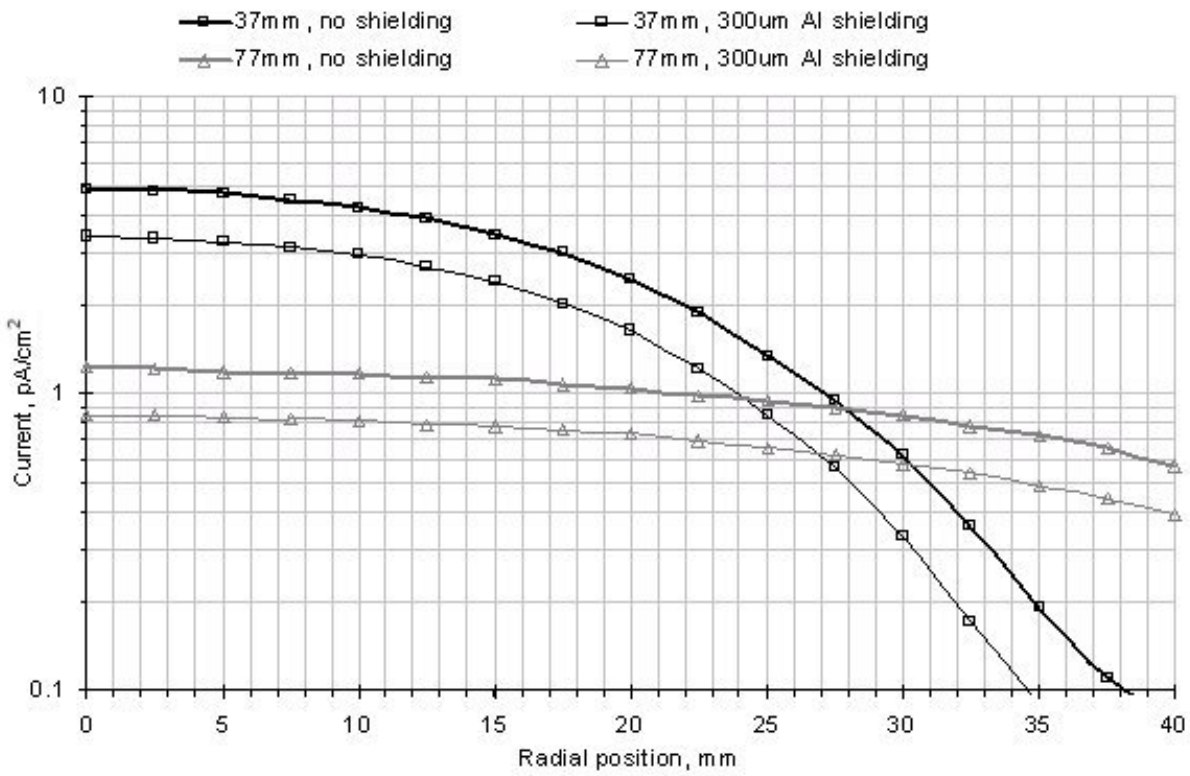

Figure 2. Measured electron current in REEF at source-sample distances of 37mm and 77mm as a function of distance from the beam axis.

Experimental Approach

Component selection

It was necessary to select a test circuit that represented generic elements of satellite electronic systems. To maximise the generality of the results the focus was placed on the so-called data, or D-type latch (also known as a flip-flop) which is a common building-block in many digital circuits. The dual CMOS latch 74HC74 was selected: in normal operation a rising edge on the clock line (CLK1/CLK2) simply latches the data at the inputs (D1/D2) through to outputs Q1/Q2. For these tests the inverted versions of Q1/Q2 (Q1' and Q2' are available on the chip) were fed back through to D1/D2 respectively (Fig. 3). This ensures that the data inputs are always different from the outputs, hence any false latch commands (i.e. CLK signals) will change the outputs and the occurrence of a false latching event is thus definitely detected. Since ESD can result in a ringing pulse with several rising edges, low pass filters with a time constant (10μs) much longer than the typical ESD duration (~100ns) were included in the feedback to prevent latch self-correction from an even number of rising edges.

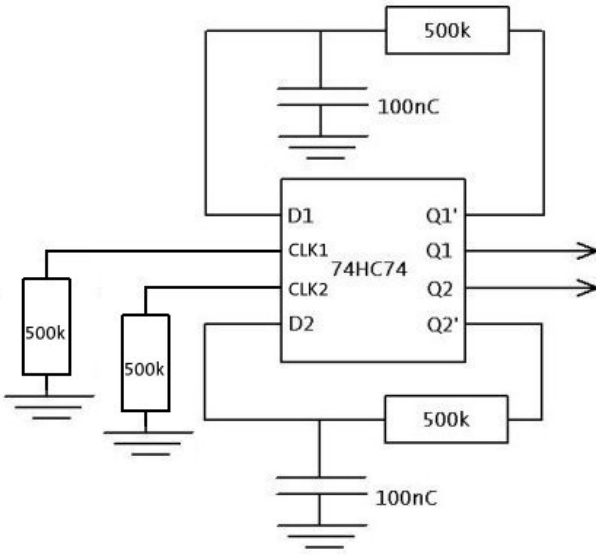

Figure 3. The circuit under test.

Circuit board and track layout

A widely used base material for space electronic circuit boards is woven glass-reinforced epoxy resin 'FR4', which has excellent electrical and mechanical properties. Because of this widespread usage and evidence from CRRES [6] which suggests that it is highly prone to generating discharges in the real space environment, FR4 was used for this work. The boards prepared had dimensions of 50mm x 50mm and two thicknesses were used: 1.6mm and 3mm. The PCB tracks were printed on one side for the circuit board using 1oz/sq. foot copper as shown in Fig. 4. A ground plane was incorporated on the rear of the PCB as this is good practice in electronic design. In fact a ground plane also has the benefit of providing a leakage path for charge stored in the board.

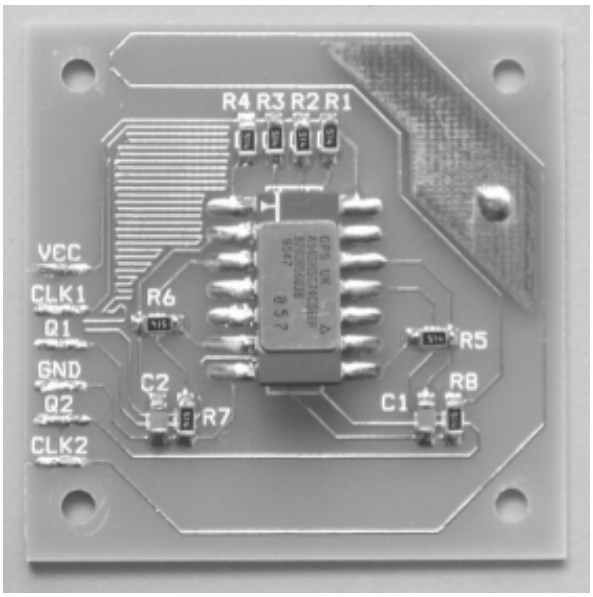

Figure 4. PCB with mounted 74HC74 chip.

There are an infinite number of possible track layouts and they strongly influence the likelihood of ESD coupling into the circuit. The board layout was relatively arbitrary except that the clock lines were made long and one clock line was routed in a wide loop whereas the other was kept to a more limited area of the board. Clock lines were pulled low via 500kΩ resistors. Another feature on the board was an island of copper, which could be left isolated if required in order to investigate the hazard that it presented. The mounting bolts could be isolated or grounded.

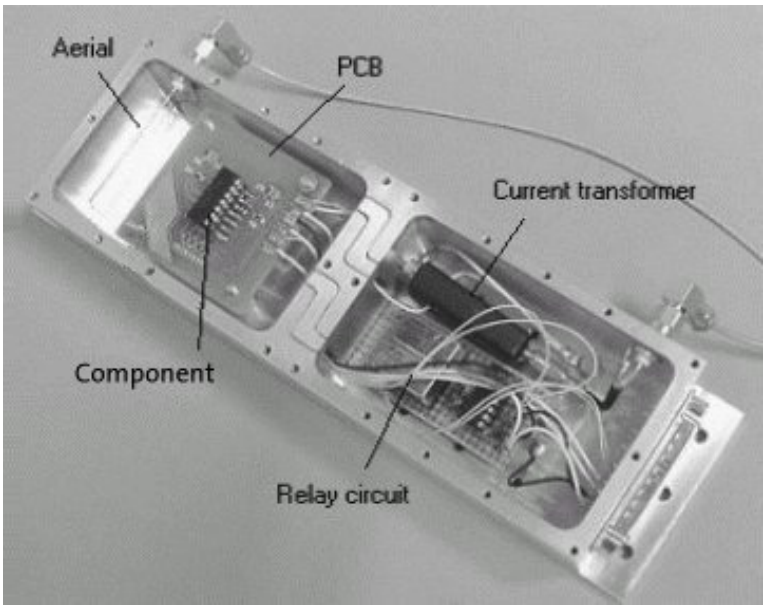

Figure 5. Test housing with all shields removed.

Installation in REEF

For the irradiations the PCB was housed in a machined aluminium box (Fig. 5) designed to mimic typical spacecraft equipment housings and surrounding structure. It is worth noting that backscatter and secondary radiation effects such as bremsstrahlung are all highly dependent on the properties of surrounding materials such as atomic number. Such secondary effects may influence the charging process. The test housing was divided into two compartments. The first compartment held the PCB under test and was positioned under the central beam axis. This compartment can be shielded using a lid if required. For the realistic experiments described below a minimal shield thickness of 300μm of aluminium was used solely to complete a Faraday cage around the sample and to maintain an even thermal environment. Note that the electron currents specified for the realistic testing are at the circuit board i.e. after the 300μm shield. Also contained in this compartment was an aerial, used to detect the occurrence of ESD, connected to a digital storage oscilloscope. The other compartment was heavily shielded and contains ancillary items (e.g. current transformer, interface for latch test circuit) which needed to be close to the D-latches to minimise the probability of noise pick up and signal attenuation. The current transformer was used to measure transients in the PCB ground plane.

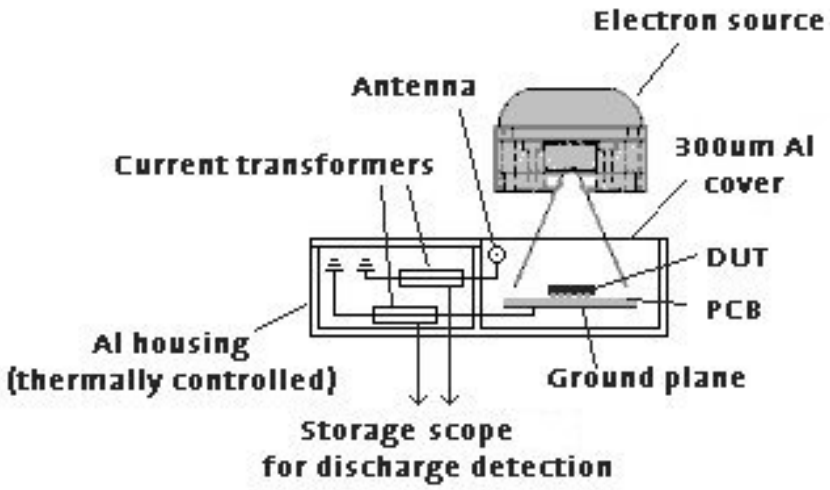

Figure 6. Schematic of the experimental arrangement.

Circuit Board Irradiations

Overview

All of the investigations used the circuit design and housing detailed above and the chip was spot shielded with 2mm of tantalum (grounded) to reduce the risk of total-dose damage. The following parameters were monitored and recorded continuously during the tests:

- Q1 and Q2 outputs to detect anomalies;
- current waveforms between PCB ground plane and ground;
- voltage waveforms from antenna;
- the DC current drawn by the circuit to check for total-dose damage.

Preliminary accelerated tests

Preliminary trials were aimed at determining whether anomalies would occur in particularly extreme (and somewhat unrealistic) circumstances, mainly as a test of the system as a whole. As such a very high (axial) electron current of ~5pA/cm^2 (incident on the PCB) was used - a level predicted for virtually unshielded components in GEO, and an order of magnitude greater than would usually be experienced by even lightly shielded (~0.5mm aluminium) components in GEO. No shield was used above the PCB. The D-latch used in this preliminary experiment was a commercial MM74HC74 device in a plastic package since it was unnecessary to risk damage to a more expensive device. The Ta shield prevented any flux reaching the chip and thus any charging of the package itself. The circuit board was made particularly susceptible to charging by:

- using a thick PCB (3mm);
- leaving metallic structures on the board (fastening bolts, isolated copper island, spot shield) ungrounded ('good practice' would be to ground such structures).

The PCB was irradiated at room temperature and the first anomaly (an uncommanded change of state of Q1 and Q2) was observed 4 hours into the irradiation and in total, 55 anomalies were observed during 231 hours of irradiation. Checks were carried out to ensure that these anomalies were not due to any type of local interference. Most of these anomalies were co-incident with large signals in both the aerial and ground plane consistent with ESD, however on two occasions these signals were measured without accompanying anomalies. After 114 hours of irradiation, the current drawn by the test circuit increased significantly and this is suspected to have been the result of ESD damage to the chip. These trials proved that electron irradiation would cause ESD and anomalies in the circuit, but under rather extreme conditions.

Realistic conditions (for GEO)

Next a set of irradiations using more realistic conditions were conducted in order to see how the rate of anomalies varied as a function of key parameters. A more typical PCB thickness of 1.6mm was used and the metallic elements (bolts and PCB floating island etc.) were grounded. The chip used was a 54HSC74 silicon-on-sapphire device from a European supplier which is frequently used on space missions. Despite being radiation-hard to 300krad(Si) the device was still fitted with a spot shield of 2mm Ta in order to avoid any possible total dose damage. The spot shield was grounded. The device came in a ceramic package and is pictured in Fig. 4. Prior to the irradiation, the board with the test components was 'baked out' at 60°C for a 24-hour period in order to remove absorbed moisture. The sample was then irradiated continuously for a period of a month without any re-pressurisation of the chamber. During this period it was subjected to a sequence of different flux and temperature conditions. Both the environment history and the latch status results are shown in Fig. 7 (lower section shows the electron current and temperature histories whereas upper section shows latch state) and summarised in Table 2. Occasionally the latch state was deliberately changed in order to test that the circuit was still functioning normally (these test flips are marked below the latch state trace in Fig. 7). A 300μm shield was used during these tests. Initially the electron current incident on the PCB was set to 0.6pA/cm^2 simulating the worst-case current predicted by FLUMIC under 0.5mm of Al which is a minimum likely shielding thickness for most spacecraft.

At room temperature (period 1 denoted P1 hereafter) no anomalies were observed but when the temperature was reduced to 0°C (P2) anomalies began occurring almost immediately. To prove that these were due to irradiation (rather than other electromagnetic interference) the source shutter was closed for a day (P3), during which time no anomalies occurred, and when it was re-opened (P4) further anomalies were seen. Over the next 12-days the temperature was initially increased to 10°C (P5) and then decreased to 0°C (P6) and -10°C (P7). It was found that the anomaly rate tended to be greatest at lower temperatures.

During 19th May the electron current was reduced to 0.14pA/cm^2 representing an average GEO level, whilst maintaining a sample temperature of -10°C (P8). Early the next day, two anomalies occurred in each channel but no further anomalies occurred over the next 4-days. It was speculated that this level was in fact too low to cause anomalies on its own but that the two anomalies that did occur were caused partly by irradiation at the higher level over previous days (during P7). When the current was again increased to the higher-level (P9)

anomalies resumed at a higher rate again. The anomalies over each period are summarised in Table 2. Note that an anomaly is defined by either of the two outputs spontaneously changing. Where both outputs changed simultaneously this is counted as only one anomaly. Test switches of the latches are excluded from the tables.

Variation in the anomaly rate for separate periods with the same current and temperature (e.g. P2, P4 & P6 or P7 & P9) was significant. This was possibly due to varying levels of residual charge from the preceding irradiation and the chaotic nature of the discharge process.

Example waveforms detected on the aerial and the ground plane are provided in Fig. 8 and Fig. 9. Virtually all anomalies were co-incident with the occurrence of such waveforms.

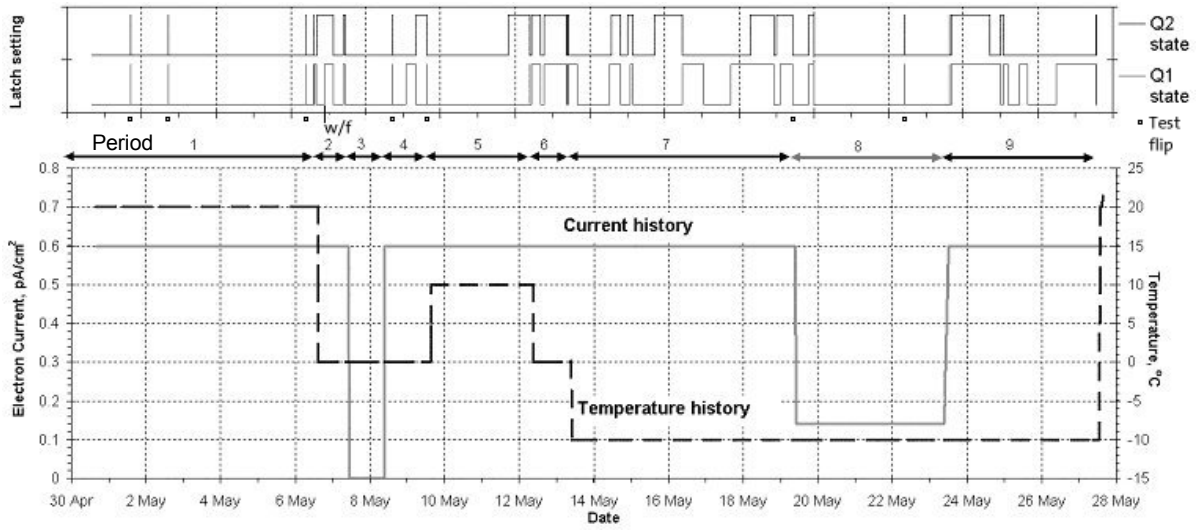

Figure 7. Test history. The top plate shows the two output states from the chip during testing. Changes in these two states represent the occurrence of anomalies (excepting tests of the normal functioning of the circuit – marked with squares below the axis). The lower plate shows the irradiation current and the temperature during the test.

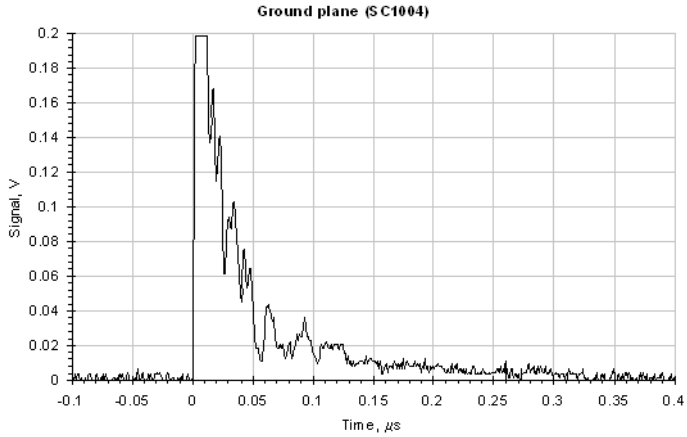

Figure 8. Typical waveform detected through the PCB ground plane (the waveform was recorded on 6th May and the corresponding event is marked by w/f in Fig. 7). The measured signal corresponds to a current from the ground plane of 0.2A/V.

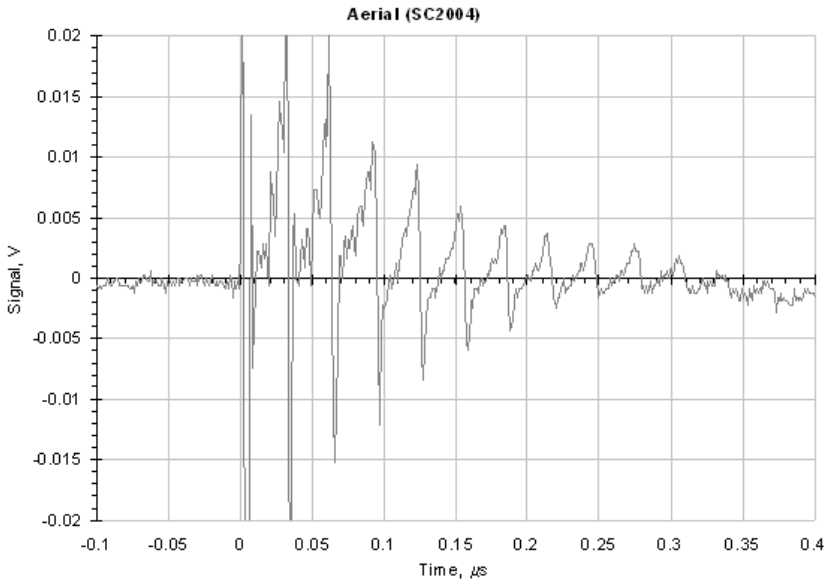

Figure 9. Typical waveform detected on the aerial (the waveform was recorded simultaneously with the ground plane waveform in Fig. 8).

Period	Temp °C	Current pA/cm^2	Time hours	Anomalies	Rate #/day
1	20	0.6	143	0	0
2	0	0.6	20	8	9.6
3	0	Shuttered	23	0	0
4	0	0.6	30	3	2.4
5	10	0.6	66	1	0.36
6	0	0.6	24	4	4.0
7	-10	0.6	136	18	3.2
8	-10	0.14	98	2	0.49
9	-10	0.6	97	8	2.0

Table 2. Summary of anomalies.

In order to examine repeatability of the results, the irradiation was repeated with a previously un-irradiated component and circuit board. All initial conditions were identical to the original test except that the initial temperature was set to –10^{o}C so it was expected that anomalies would occur readily. The recorded latch outputs (Q1 and Q2) and the temperature and current histories are shown in Fig. 10. Markers below the trace again denote test flips (non-anomalous events) in the latch trace.

Conditions were maintained at a constant level for the first period of the investigation which lasted approximately 7 days. However, during this period, no anomalies occurred in the system. The decision was thus made after seven days to increase the irradiation current by a third (to 0.8pA/cm^2). Again, over the next 24 hours, the circuit again showed no signs of circuit anomalies or ESD events. A third period was thus undertaken for which the temperature was reduced to –20^{o}C. The effect of this temperature reduction was immediate. Within 40 minutes of the reduction, an ESD event was recorded coinciding with changes of both Q1 and Q2. A total of 19 anomalies were observed in the circuit during the 23 hours

proceeding the change in temperature, seven of which could be directly associated with ESD events. A summary of this test is provided in Table 3.

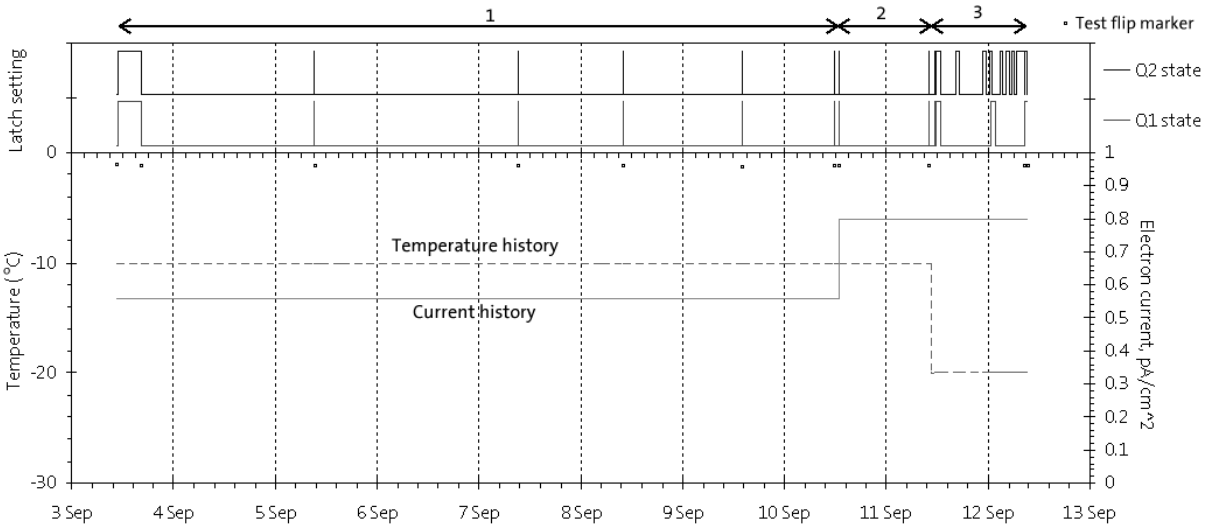

Figure 10. Test history of second test. The top plate shows the two output states from the chip during testing. Changes in these two states represent the occurrence of anomalies (excepting tests of the normal functioning of the circuit – marked with squares below the axis). The lower plate shows the irradiation current and the temperature during the test.

Period	Temp °C	Current pA/cm^2	Time hours	Anomalies	Rate #/day
1	-10	0.6	170	0	0
2	-10	0.8	22	0	0
3	-20	0.8	23	19	19.8

Table 3. Summary of anomalies in second test

Conclusions

It has been shown that anomalous changes of state can occur in a simple digital latch mounted on an FR4 board when irradiated in a close approximation of the worst-case (electron) environment expected in GEO under 0.5mm of aluminium shielding. In view of the co-incident transients detected by the antenna and ground-plane current monitor these anomalies are concluded to be due to electrostatic discharges occurring either on or within the PCB (there were no ungrounded metallic elements). Reducing the flux to near-average GEO intensities (at constant temperature) resulted in a much reduced anomaly rate compared to the worst-case flux, as would be expected.

It had been expected that the anomaly rate would increase at lower temperatures since dielectric conductivity reduces sharply with temperature [8]. Our results support this prediction to some extent, however there seems to be an important and unexpected effect resulting from (rapid) changes in temperature which, in both experiments, led to a sudden onset of discharge events. Further investigation is desirable to confirm this observation and determine its significance for spacecraft.

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