LABORATORY EXPERIMENTS ON MITIGATION METHODS AGAINST SOLAR ARRAY ARCING: PREVENTION OF ION CHARGING

Mengu Cho, Ko Shiraishi, and Masayuki Hikita

Kyushu Institute of Technology, Tobata-ku, Kitakyushu, 804-8550, JAPAN

phone&fax: +81-93-884-3228, cho@ele.kyutech.ac.jp

Abstract

When a solar array has a high voltage in Low Earth Orbit, an arc occurs. It causes surface degradation, electromagnetic interference and other undesired side-effects. Following three mitigation techniques to suppress the arcing are tested in laboratory experiments. (1) PET (polyethyleneterephthalate) film in front of the coverglass to physically prevent the charging by ions. (2) Conductive wire in front of the interconnector to narrow the sheath region around the interconnector, also to prevent diffusion of the discharge plasma. (3) Conductive coating coverglass. Advantages and disadvantages of each method is discussed.

1. Introduction

The use of high power in future space missions calls for high voltage power generation and transmission to minimize the energy loss during power transmission and the cable mass. In order to promote industrial use of Low Earth Orbit (LEO), such as manufacturing, sight-seeing, or power generation, the power of a large LEO platform after the International Space Station (ISS) will soon reach the level of MW. In principle, the transmission voltage scales to the square root of the power to be delivered. Therefore, in order to realize a MW-class space platform, the power must be delivered at least 400 volts. In order to realize 400 volts operation in LEO, arcing caused by interaction between the spacecraft and the surrounding LEO plasma must be overcome.

When a solar array generates the electricity, most of the voltage becomes negative with respect to the the surrounding plasma due to mass difference between ions and electrons. Positive ions impact on coverglass surface and charge it positively. Then the electric field near triple junction, where interconnector (conductor), adhesive (dielectric) and vacuum meet together as shown in Fig. 1, is enhanced and an arc occurs.

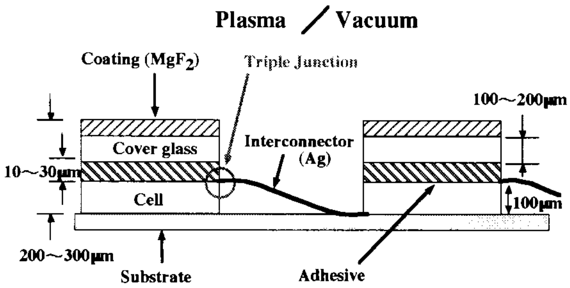

Figure 1: Schematic picture of solar array structure near interconnector

There have been numerous studies on arcing on high voltage solar array in LEO condition since 1970s, such as Refs. [1, 2]. It is now known that an arc occurs once an array has a negative potential as low as -100V with respect to plasma. Repeated arcs lead to surface degradation. Electromagnetic interference due to the arc current is another concern. Moreover, a single arc might shorten the array circuit and lead to permanent loss of the array power, which is believed to be the cause of the failure of Tempo-2 [3].

The purpose of the present paper is to study mitigation methods against the arcing. The basic strategy is to avoid the charging of coverglass surface due to the surrounding plasma. We consider the following three methods in this paper;

1. Transparent film is placed over the array so that it physically blocks ions from charging the coverglass surface.

2. A conductive wire is placed over the interconnector so that it shrinks the electrical sheath to collect ions from the ambient.

3. Conductive coating is made on coverglass surface so that the coverglass surface becomes the

Proc. 7th Spacecraft Charging Technology Conference, 23-27 April 2001, ESTEC, Noordwijk, The Netherlands. ESA SP-476, November 2001

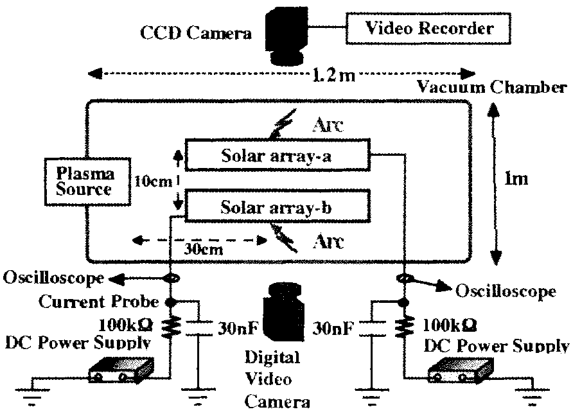

Figure 2: Schematic picture of experimental set-up

same potential as the interconnector.

The first method has an advantage that it can sustain the thermal cycle in orbit. If we put insulator coating directly on the interconnector surface, it often leads to crack due to the thermal cycles in orbit. There is also a report of PASP space experiment [4] that an array with solar concentrator had less arc compared to other designs. Probably the concentrator lens had the similar effect as the film. In the present paper we confirm that point by laboratory experiments. The second method has an advantage that it can minimize the loss of power output compared to the first one, because the decrease of received sun light due to thin wire is negligible. The third method has an advantage that the conductive coverglass is already in use in real spacecraft. Therefore if this method works, no design change is necessary for the high voltage power generation. We test the three methods via laboratory experiment where the LEO plasma condition is simulated. In the second part of this paper, we describe the experimental method. In the third part we present the experimental result and compare the three methods. In the fourth part we conclude this paper.

2. Experiment

Figure 2 shows the schematic of experimental setup. The plasma chamber is a cylinder of $1m$ diameter and $1.2m$ length. The chamber is filled with Ar plasma made by a Kaufman-type plasma source. The typical chamber conditions during the experiment is $7.0 \times 10^{-4} Torr$ as the gas pressure, $5 \times 10^{-11} m^{-3}$ as the plasma density, and $1.5eV$ as the electron temperature.

In Fig. 3 we show a photograph of solar array used in the experiments. This is a solar array of conventional design, which consists of six $2cm \times 4cm$ silicon solar cell connected in series. Cells are glued on

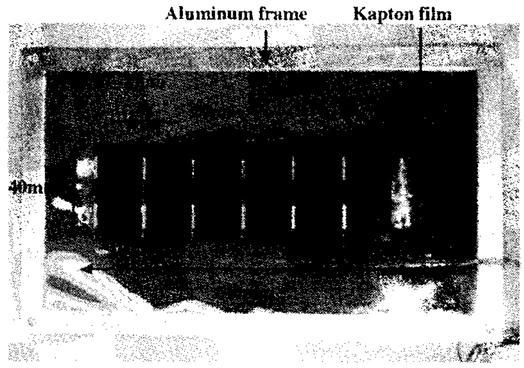

Figure 3: Photograph of solar used in the experiments

Kapton film via RTV silicon and the film is held by an aluminum frame. Figure 1 shows the schematic of close-up near the interconnector. We apply the mitigation techniques to this array and place two arrays in the plasma chamber at the same time. Different degree of mitigation is applied to the two arrays so that by comparing the two, we can measure the effect of the mitigation methods. The two arrays are placed back-to-back so that the array surface is parallel to the chamber axis and the coverglass faces outward. Each array is biased by a DC power supply (Takasago, TMK1.0-50) to a negative potential from $-100V$ to $-1000V$ for the duration of 10 minutes or 20 minutes. During the experiment, the bias voltage is increased in time, *i.e.* more negative. The capacitance shown in Fig. 2 provides the charge to the arc current, which simulates the coverglass of other parts of solar array in real spacecraft.

The solar array surface is monitored by a video camera so that the arc point is identified from the optical flash observed at the arc onset. The array potential is monitored by a high voltage probe (Sony Tektronix P5100) and the arc current is monitored by a current probe (Sony Tektronix P6022). The probe signals are connected to a digital oscilloscope (Sony Tektronix TDS224). By integrating the current waveform with respect to time, we calculate the electrical charge flown in each arc. For all the cases, the oscilloscope is triggered by a sudden jump in the array potential at the arc onset.

We carried out 7 cases of experiment. For cases 1, 2, and 3, we tested an array (SA-1b, SA-2b, SA-3b) with a roof made by PET film which is separated by the distance L as shown in Fig. 4 The other array (SA-1a, SA-2a, SA-3a) has no roof which is used as a reference (see Fig. 3). The reason why we select PET film is simply because it is easy to obtain. The film used in the experiment is $100\mu m$ thick overhead-projector sheet sold at any office supply shop. When we select the material used in orbit, it must

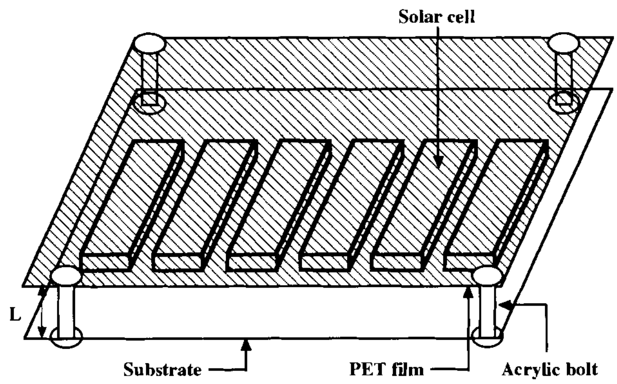

Figure 4: Schematic picture of array with PET film over solar array (SA-1b, SA-2b, and SA-3b). The thickness of PET film is $100\mu m$ and the distance between the array and film is defined by L.

be transparent, thin, and resistive to radiation and atomic oxygen. Ions still charge the coverglass by entering through the gap between the film and the coverglass. To see at what gap distance, L, we can prevent the ions entering the gap, we vary L in cases 1,2, and 3. We vary the gap by adjusting acrylic bolts and nuts at the four corners of the aluminum frame.

In case 4, both arrays are covered by the PET film. The PET film of one array (SA-4a) has a square hole ($5mm \times 10mm$) over the cable junction which is shown as a shaded square in Fig. 5. The other array (SA-4b) has a square hole ($5mm \times 10mm$) over an interconnector as shown in Fig. 5. An arc on solar array occur mainly at three different parts, interconnector between coverglasses, cable junction, and edge of cells on Kapton film. When the array is covered by PET film with an hole, most of arcs occur at the hole. By having opening at the two different parts, we investigate the dependence of arc occurrence on the position on solar array.

In case 5, both arrays are covered by the PET film. One array (SA-5a) exposes most of the array area except the cable junction as shown in Fig. 6. The other array (SA-5b) has 4 square holes, ($5mm \times 10mm$, each). In real solar array, it is relatively easy to insulate the cable junction from the plasma, such as EOS-AM array [5]. Therefore, having cable junction covered by PET film simulates more realistic situation. The several holes are made on SA-5b to simulate the debris or micrometeoroid impact on the array which is inevitable during the long time operation in space. The design of SA-5a is also used as a reference in cases 6 and 7 (SA-6a, SA-7a).

In case 6, one array (SA-6b) has tin-plated conductive wire ($0.5mm$ diameter) over the interconnector at a height of $5 \sim 7mm$ as shown in Fig. 7. The conductive wire is grounded. When an interconnector with a negative potential is exposed from the gap between coverglasses, it extends electric sheath outward to collect ions from the ambient plasma [6]. Some of ions attracted by the sheath hit the edge of coverglass and charge it positively. By placing the conductive wire, we can limit the expansion of sheath and slow the charging of the coverglass.

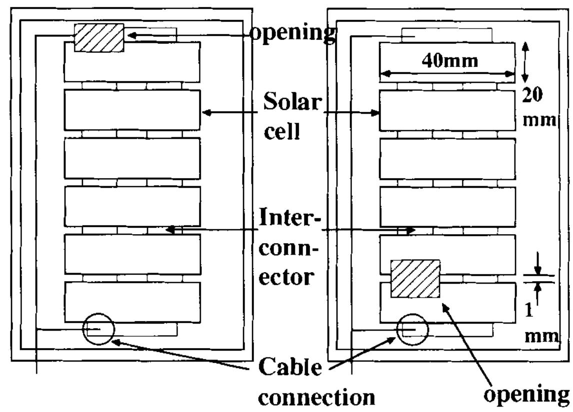

Figure 5: Schematic picture of array used for case 4 in the experiment. Left; SA-4a, Right; SA-4b. The shaded square indicates a hole exposing underlying triple junction. The PET film is placed on the arrays with no gap, *i.e.* $L = 0$. The experiment is carried out four times.

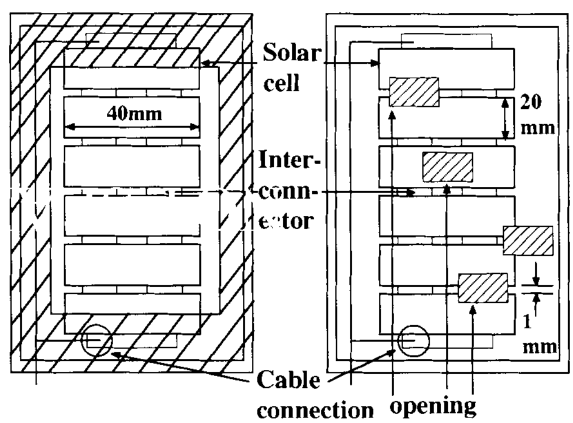

Figure 6: Schematic picture of array used for case 5 in the experiment. The shaded area of the left, SA-5a, indicate PET film, which exposes most of array to the plasma except the cable junction. The shaded area of the right, SA-5b, indicates holes in PET film exposing the underlying triple junctions. The PET film is placed on the arrays with no gap, *i.e.* $L = 0$. The experiment is carried out three times.

In case 7, one array (SA-7b) has coverglass which is coated by transparent conductor, ITO (Indium Tin Oxide), whose thickness is $20nm$, (see Fig. 8). We

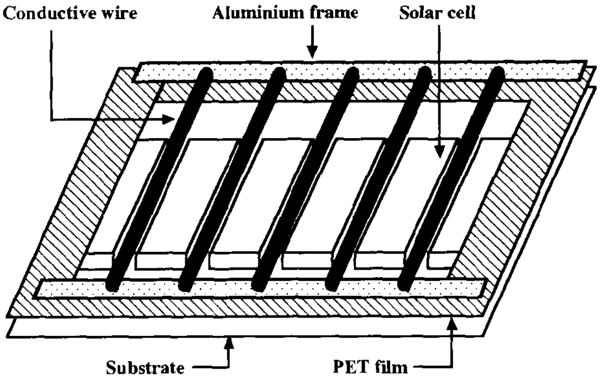

Figure 7: Schematic picture of array, SA-6b, used for case 6. The conductive wire is over interconnectors at the height of 5 $\sim$ $7mm$. The wires are grounded through the aluminum frame. PET film is also placed with $L = 0$ to hide the cable junction from the plasma. The experiment is carried out three times.

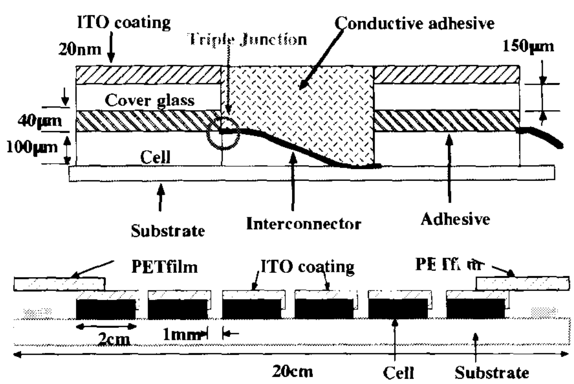

Figure 8: Schematic picture of array used for case 7 in the experiment; Close-up view near interconnector (upper) and whole view of array, SA-7b, (lower). The ITO coating is connected to the interconnector via conductive adhesive. PET film is also placed with $L = 0$ to hide the cable junction from the plasma. The experiment is carried out three times.

use a conductive adhesive (Aquadug^{TM}), to make the ITO surface the same potential as the interconnector. In this way, no field intensification occurs at the interconnector surface.

3. Experimental Results and Discussion

Figures 9 and 10 show the arc rates against the bias voltage. Each bias voltage was applied for 10 minutes. When the gap between the film and array surface was sufficiently narrow, the array with film (SA-b) had less arc rate than the array without film (SA-a). As the gas became narrower, the amount

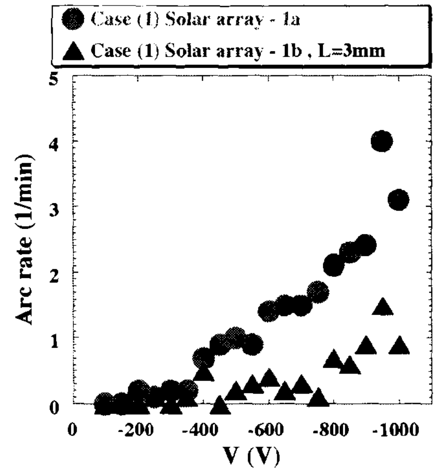

Figure 9: Arc rate for different bias voltages measured in case 1.

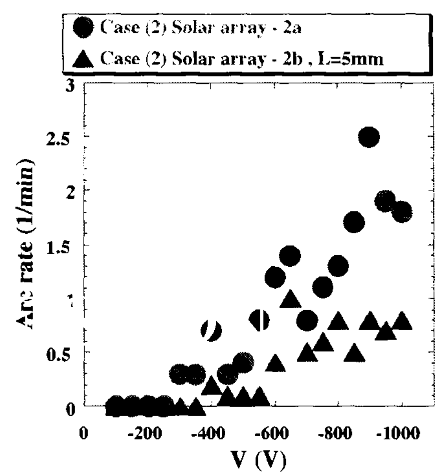

Figure 10: Arc rate for different bias voltages measured in case 2.

of positive ions penetrating the gap decreased and the coverglass was charged less. For the case of $L = 10mm$, no significant difference was observed between SA-3a and SA-3b. Figure 11 shows the points of arc occurrence identified from the video image. The vertical and horizontal axis of Fig. 11 corresponds to pixels. Among 73 arcs observed by the oscilloscope, 23 arcs were identified from the video image. Most of arcs occurred at the edge of solar cells, which was consistent with the idea that positive ions penetrating the gap charged the coverglass surface. The reason why the arcs concentrated to the upper portion of the array is unknown for the moment. Possible explanation is that the gap was slightly wider at the upper part. The accuracy of the gap separation was $\pm 1mm$.

We carried out 4 experiments for case 4 and saw

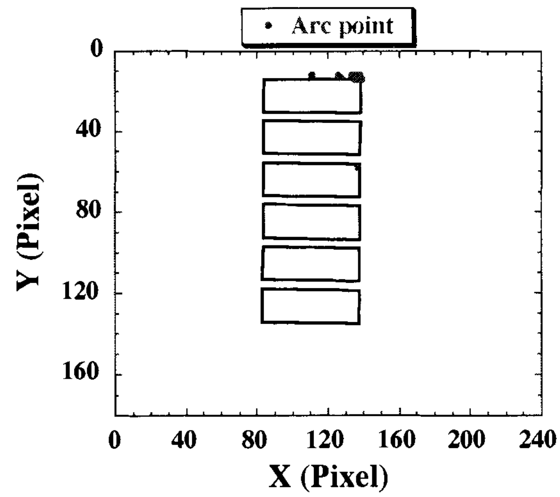

Figure 11: Location of arcs identified from the video image of SA-1b. Locations of 23 arcs were identified, though 73 arcs were measured by the oscilloscope. The six squares drawn in solid lines indicate coverglass.

no significant difference between SA-4a and SA-4b. The arc rates differed only by ±12% at maximum. We also compared the charge flown at each arc, but the difference was within ±15%. Therefore, as long as a triple junction is formed and exposed to space, either interconnector or cable junction, an arc occurs and once an arc occurs its scale is similar. The triple junction at the cable junction is formed by the electrode surface and the adhesive covering the cable.

Figure 12 shows the arc rate against the bias voltage for case 5. Three experiments are combined to increase the denominator of the arc rate. The bias voltage is applied for 20mins at -300V, 40 mins at -400V, 50mins at -500V, and 60mins at -600V or higher. The arc rate is calculated by dividing the total number of arcs in the three experiment in the total biasing time. The array with few holes in PET film (SA-5b) has far less arc rate than SA-5a. This is because the length of exposed triple junction of SA-5b is much shorter than SA-5a. Therefore, even if holes are produced on PET film during long operation in space, the mitigation effect does not decrease drastically.

Figure 13 shows the arc rate for case 6. The array with conductive wire (SA-6b) has less arc than the normal design (SA-6a). There are two reasons why the arc occurred less at SA-6b. One reason is that the presence of conductive wire with zero potential limits the expansion of the ion collecting sheath from the interconnector. The result of field calculation shows that the sheath is indeed suppressed for SA-6b compared to SA-6a. The other reason is

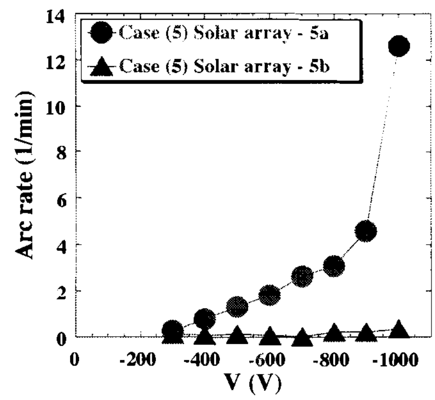

Figure 12: Arc rate for different bias voltages measured in case 5.

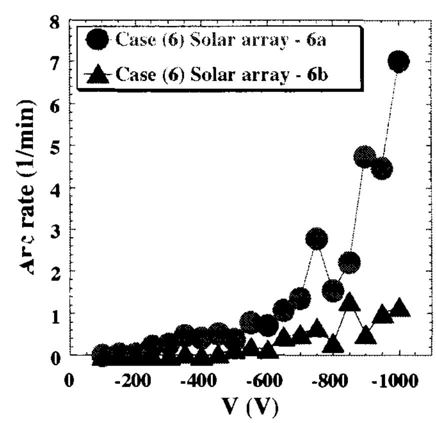

Figure 13: Arc rate for different bias voltages measured in case 6.

that the conductive wire absorbs the arc plasma before it spreads inside the chamber. The charge flown in one arc for SA-6b is 2/3 of the charge for SA-6a. When an arc occurs, the arc plasma is ejected and the plasma density increases locally. The enhanced plasma density increases the arc rate as some of ejected charged particles recharge the coverglass.

In case 7, there was no significant difference regarding the arc rate between SA-7a and SA-7b. Above -600V, SA-7b which had conductive coverglass had even higher arc rate than SA-7a. The charge flown in one arc was more or less same, within ±9.1% difference, for the two arrays. Before the experiment, it was expected that the conductive coverglass significantly suppress the arc occurrence because no field enhancement should have occurred at the interconnector. The video image was analyzed and the locations of 134 arcs were identified among 146 arcs observed by the oscilloscope. Figure 14 shows the distribution of the arc points. Arcs oc-

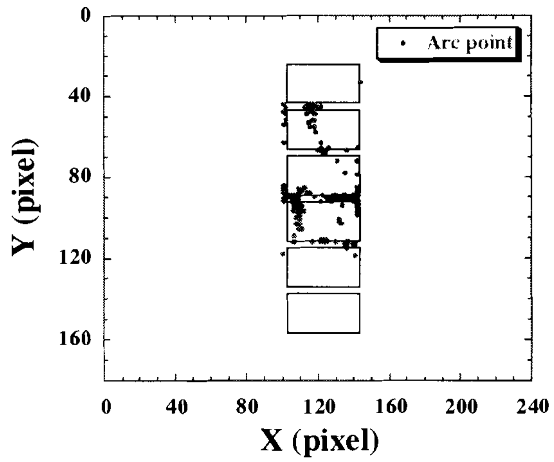

Figure 14: Location of arcs identified from the video image of SA-7b. Locations of 134 arcs were identified, though 146 arcs were measured by the oscilloscope. The six squares drawn in solid lines indicate coverglass.

curred mostly between the third and fourth cells. They occurred even on the coverglass surface.

As we look at the temporal development of the distribution, arcs first occur at the edge of solar cell, where the triple junction is formed by a solar cell and adhesive on Kapton film. Once an arc occurs, a large current flows into the arc point and the conductive coating near the arc spot is deteriorated and sputtered out due to interaction with the dense arc plasma. Once the thin conductive coating is removed and the underlying dielectric surface is exposed, new triple junction is formed by the remaining conductive layer, the dielectric surface, and space. Then, once an arc occurs, there is a possibility that arcs occurrence is accelerated as the nearby conductive coating is removed. Therefore, even if we can suppress arcs at interconnector, as long as other triple junction remains, such as the solar cell edge, the conductive coating alone cannot suppress the arcing completely.

The inspection of the ITO layer after the experiment showed that the resistance of coverglasses from the second to fifth one (four inner ones in Fig. 14) increased to several $M\Omega$, although the resistance before the experiment had been only several $k\Omega$. The four coverglasses also discolored. The first and sixth coverglass where few or no arc occurred showed little change in the resistance and color. We also investigate the interconnector between the third and fourth cells in Fig. 14 via 60× microscope. The conductive adhesive used to connect the ITO layer and the interconnector showed significant degradation and some part were completely removed. Between the fifth and sixth cells, no change was observed.

4. Conclusion

When an solar array generates the power at a voltage higher than 100V in Low Earth Orbit plasma environment, an arc occurs due to field intensification at the triple junction through interaction with the space plasma. We have carried out laboratory experiments to develop a solar array which is capable of generating the power at $1kV$. Three mitigation techniques have been tested.

Placing transparent film over the interconnector to physically block ions to charge the coverglass has shown a good result to suppress the arc occurrence if the gap between the film and the array surface is sufficiently narrow. Placing conductive wire over the interconnector also showed a good result to suppress the arc occurrence. The installation, however, looks very difficult, because once the wire touches the interconnector it automatically shorten the array circuit. The results of conductive coverglass has been very disappointing. If the triple junction formed by the solar cell edge and the insulator film on the substrate can be hidden from the plasma, the use of conductive wire has a good potential as the arc suppression. As long as the cells are glued on insulator film, however, the triple junction at the cell edge is difficult to avoid.

As a future study, the use of transparent film should be investigated further. If we can find material which is transparent and resistive to radiation and atomic oxygen, this method looks very promising. How to install such film on the real solar array is another issue to be investigated in the next study.

5. Reference

1 Hastings D. E. *et al.*, *J. Spacecraft Rockets*, 29(4), 1992. pp.538-554.

2 Ferguson D. C. *et al.*, AIAA paper 99-0218

3 Katz, I. *et al.*, AIAA paper 98-1002

4 Guidice, D. A. *et al.*, AIAA paper 96-2331

5 Davis, S. *et al.*, SAE Tech. Paper 1999-01-2582,

6 Cho, M. *et al.*, *J. Spacecraft Rockets*, 28(6), 1991. pp.698-706.